EEUG News

The newsletter for Educational Electronic Computer Aided Design users

Volume 11 No 1 July 1998 Editor: Steve Quigley (S.F.Quigley@bham.ac.uk)

News from the ECAD Educational User Group Committee

In this issue

CHAIRMAN'S WELCOME.

Welcome to the latest edition of the EEUG Newsletter.

As you will see from elsewhere in this newsletter there has been a number of changes in personnel on the EEUG Committee. As a consequence of Chris Harrison moving out of the Higher Education environment he had to relinquish the post of treasurer before the end of his due time on the committee. In order to provide continuity, Steve Harrold kindly volunteered to take over the finances of EEUG and so stepped down as Chairman. Dave Vallis agreed to continue his work as Secretary as did Steve Quigley as Newsletter editor. That left myself as the only other "old hand" (just!) and so I took on the job of Chairman.

I should personally like to thank Chris for his contribution as Treasurer and the others for continuing to serve on your committee. As you will see elsewhere there is much new blood with four additional members and I wish to welcome them all.

The committee exists to serve the members of EEUG and to represent your views so it is important that you inform us of any issues in ECAD that concern you. I would encourage you to get in touch and let us know what you think. In particular, Jon Travis and myself should be made aware of any points that relate to the RAL support services.

The January workshop in Oxford, "Teaching Design", very ably organised by John Lidgey and his team, was technically very successful and two of the founder members of EEUG (Peter Jones and Erik Dagless) were on hand to cut the 21st birthday cake. Unfortunately the level of support by members was again disappointing but despite this the AGM decided to continue with two meetings a year, but to keep the situation under review, particularly as academic teaching

Only one copy of this newsletter is sent to each institution, so please circulate it to all those who may find it useful

patterns change. I therefore urge you all to attend the September meeting at the University of Sussex in Brighton where the sun always shines and the beach is near at hand! I look forward to welcoming you.

Dr Mike English
School of Engineering
University of Sussex, Brighton
(m.j.english@sussex.ac.uk)

THE COMMITTEE

The new star-studded cast is:

Chair: Mike English (m.j.english@sussex.ac.uk)
Secretary: Dave Vallis (d.j.vallis@open.ac.uk)
Treasurer: Steve Harrold (s.harrold@umist.ac.uk)
Newsletter Editor: Steve Quigley (s.f.quigley@bham.ac.uk)
Other committee members:
Tim Forcer (tmf@ecs.soton.ac.uk)
Margaret Fraser (m.l.fraser@rgu.ac.uk)
David Holding (d.j.holding@aston.ac.uk)
Jon Travis (j.r.travis@shu.ac.uk)

Mike English and Jon Travis are the RAL MSC Advisory members together with Phil Hallam who continues until 1999.

EDEC UPDATE

The Electronic Design Education Consortium (EDEC) was set up in 1992 with the aim of developing a range of Computer-Based Learning software for use in the education of undergraduates in electronic engineering and computer science. The project has received over £1M of funding from the Higher Education Funding Councils through the Teaching and Learning Technology Programme (TLTP) and more than 150 hours of material are now available in the following four subject areas:

- *Electronic Circuit Design*
- *Digital Design*
- *System and High-Level Design*
- *Testing and Design for Test*

Full details of the syllabus and short demos of the interactive methods used can be found on the EDEC website:

http://edec.brookes.ac.uk

Many universities and colleges in the UK received preliminary versions of the EDEC courseware when the first phase of the project was completed in 1995. Since then a great deal of effort has been put into testing and developing the courseware to iron out any bugs and errors and generally improve the quality of the finished product. This second phase of the EDEC project is ongoing since the courseware is being continually modified to ensure that it is up-to-date and capable of running on the latest PCs and operating systems. The EDEC subscription scheme was launched in 1996 to enable this work to carry on and EDEC Multimedia Ltd. was established to develop a sales and marketing plan for the courseware in industry and in countries outside of the UK. So far over 35 UK HE institutions have decided to join the EDEC subscription scheme which provides a site licence for use of the latest version of the courseware as well as access to the latest updates and full product support.

Version 3.0 of the EDEC courseware is now available on CD-ROM and includes the most up-to-date versions of all of the EDEC modules that have so far been released, plus several new modules that were previously only available for trial on the web. Also included in version 3.0 are the EDEC launchers, which enable all of the courseware modules to be started from one icon and all of the workbooks to be accessed from another. EDEC is also distributing with the version 3.0 CD-ROM another disk containing courseware that has been developed as a result of

collaboration between EDEC and a consortium of Polish universities under an EC-funded TEMPUS programme. This additional material covers a range of topics including image processing, graphics, networking, reliability, computer architecture/DSP, neural networks and VHDL. The TEMPUS CD-ROM in its preliminary (beta release) form is being distributed free of charge to EDEC subscribers for evaluation purposes, pending a decision being made about its incorporation into the official EDEC portfolio.

For UK higher education institutions the cost of joining the EDEC subscription scheme is £500 per annum which includes a copy of the latest (version 3.0) CD-ROM, access to updates on the WWW and full product support. Any university wishing to join the scheme should use the order form available on the EDEC web site and send it with an official order or a cheque for the above amount to Dr. Peter Jones at the University of Manchester (the full address is given on the web pages).

Finally, EDEC is pleased to announce that it has recently been successful in a bid for further funding under phase 3 of the Teaching and Learning Technology Programme. The aim of this latest phase of the project is to integrate the EDEC material into existing course structures and to evaluate the cost effectiveness of using educational technology. Key features of this work will be an investigation of web-based delivery frameworks and flexible approaches to the configuration of courseware. EDEC subscribers will be kept fully informed about the progress of this work and will also be given the opportunity to obtain pre-release versions of material produced as part of the project. More details will be presented as part of the EDEC update session to be held at the next EEUG Workshop in Sussex in September.

Peter Hicks (p.hicks@umist.ac.uk)

USEFUL WWW SITES

By now, I doubt any electronics company is without a Website. Many publicise these in their literature. If you are looking for a particular company, say SuperFPGA, then trying <http://www.superfpga.com> will normally get you onto the company's home page. This doesn't always work, and there are two main problems. First, some URLs were registered by entrepreneurs hoping to sell them on to the big boys. Sometimes this was successful, more often the large company simply registered something slightly different. The second problem is that the page you get may be the corporate home page - sometimes based in Japan - and it may take a while to work through the heirarchy to get to the technical information you seek. In cases like these, I recommend using either your favourite search engine (mine is Alta Vista <http://www.altavista.com>) or a reference site consisting mainly of links, such as Chip Directory <http://www.xs4all.nl/~ganswijk/chipdir/chipdir.html> (or its UK mirror site <http://www.shellnet.co.uk/chipdir/chipdir.htm>). These approaches work equally well for semiconductors, software and equipment.

Where one is seeking generic or support information, life can get a bit difficult. Ultimately, the only solution is taking the time to build up a stock of "bookmarks" for useful sites - particularly those which themselves maintain ordered sets of links. The list on the next page is extracted from my personal bookmark file, and is neither exhaustive nor comprehensive - just a set of starting points that I've found useful. Given the rate at which things change in the WWW, it will probably be inaccurate by the time you read this!

Happy surfing!

Tim Forcer
Dept of Electronics and Computer Science,
University of Southampton,
tmf@ecs.soton.ac.uk

LIST OF USEFUL WWW SITES

Name	URL	Notes
101 Computer Hardware Links	<http://www.sharewareplace.com/101/101hard.shtml>	Like it says!
The Hardware Book	<http://margo.student.utwente.nl/stefan/hwb/hwb.html>	Connector pinouts, cables, adaptors
IEEE 1284	<http://www.fapo.com/ieee1284.htm>	The PC parallel port.
Tomi Engdahl's PC hardware page	<http://www.hut.fi/Misc/Electronics/pc/>	Buses, drivers, components.
The ECAD Initiative	<http://www.asd.rl.ac.uk/msc/ecad.html>	At RAL - but you knew about this anyway?
Educational ECAD User Group	<http://www.cs.rhbnc.ac.uk/eeug/eeug.html>	At Royal Holloway. Official, but very out of date.
Circuit Cookbook	<http://www.ee.ualberta.ca/~charro/cookbook/>	Archive of useful stuff, plus some links.
CircuitOnline	<http://www.circuitonline.com/>	Directory of links. Commercial.
Data Bookshelf	<http://homepage.cistron.nl/~nctnico/databook.htm>	Directory of links for data sheets.
US Patent and Trademark Office	<http://patents.uspto.gov/>	Searchable for full details of all US patents since 1976, ***free***.
University of Nebraska-Lincoln	<http://www.engr.unl.edu/eeshop/proto.html>	Useful set of notes titled "Electronic Prototyping: Tips and Pitfalls".
Alex's Electronic Test Bench	<http://www.iserv.net/~alexx/>	Pages of links.
Circuit Schematics	<http://www.web-span.com/pjohnson/schematics.htm>	Links to Websites of schematics.
Chu's Guide to Microprocessors	<http://www.wmin.ac.uk/~nguyenc/MPA.html>	Comprehensive information and links.
comp.arch.fpga archive	<ftp://www.super.org/pub/www/FPGA/caf.html>	Structured archive of the programmable logic newsgroup.
File formats	<http://toleak.etec.wwu.edu/IntrolDoc/Reference/formats.html>	All those data file formats for EPROMs, PLDs etc.
FPGA related WWW Links	<http://www.mrc.uidaho.edu/fpga/fpga.html>	Structured directory of links to companies and resources.

Educational ECAD User Group Workshop
University of Sussex
9th - 10th September 1998

The 22nd EEUG Workshop will be held at the University of Sussex at Brighton on the 9th and 10th of September 1998. The topic for the workshop is "Design Entry – HDLs vs. Schematics" and it will discuss the relative merits of the two approaches for teaching and research.

Presentations have been confirmed from:

- Tim Forcer, University of Southampton: "HDLs in an Electronics degree course – a systematic progression"
- Jonathan Bromley, Oxford Brookes University: "Learning from the Softies"
- David Holding, Aston University: "Introducing VHDL design case studies in EE degree programmes"
- Jim Proudfoot, University of Wales, Swansea: "Design Entry vs. Resourse Utilisation in Altera Max+ plus"
- Iakovos Stamoulis, University of Sussex: "VHDL design flow for computer graphics ASICs & FPGAs"

After dinner on the Wednesday evening Darren May of ALT Technologies Ltd will present a short lecture and demonstration of *Synplicity*. The Rutherford Appleton Laboratories will be demonstrating PC tools during coffee breaks and over lunch on the Thursday. The workshop will also include the usual update sessions on EDEC, RAL and Liaison committee business.

The cost for overnight attendees will be £66, which includes dinner and accommodation on the 9th and breakfast, lunch, tea and coffee on the 10th. The cost for attending only for the day on the 10th will be £30, which includes lunch, tea and coffee.

Please post or email the following form, with payment documentation, to the EEUG Treasurer (s.harrold@umist.ac.uk), in order to register for the workshop.

Please circulate this information to your colleagues. We hope you will be able to join us.

Dr Mike English
(on behalf of the EEUG committee)

Educational ECAD User Group Workshop

University of Sussex, Brighton

9/10 September 1998

Programme

Weds 9 September

7.00 pm	Dinner
8.30 pm	Lecture and demonstration of *Synplicity* by Darren May of ALT Technologies Ltd
	Bar

Thurs 10 September

8.45 a.m.	Registration
9.15 a.m.	Chairman's Welcome - *Mike English (Sussex)*
9.20 a.m.	HDLs in an Electronics degree course – a systematic progression *Tim Forcer (University of Southampton)*
9.45 a.m.	Learning from the Softies *Jonathan Bromley (Oxford Brookes University)*
10.10 a.m.	Introducing VHDL design case studies in EE degree programmes *David Holding (Aston University)*
10.35 a.m.	Coffee and RAL Roadshow
11.05 a.m.	Design Entry vs. Resourse Utilisation in Altera Max+ plus *Jim Proudfoot (University of Wales, Swansea)*
11.30 a.m.	VHDL design flow for computer graphics ASICs & FPGAs *Iakovos Stamoulis, (University of Sussex)*
11.55 a.m.	EDEC Update *Peter Hicks (UMIST)*
12.20 p.m.	RAL Roadshow & Lunch
2.15 p.m.	RAL Software Support update - *Dr John McLean (RAL)*
2.40 p.m.	Liaison Committee Report
3.00 p.m.	Tea & Close

For Registration details please contact Dr S. Harrold (s.harrold@umist.ac.uk) or Dr M.J. English (m.j.english@sussex.ac.uk).

Educational ECAD User Group Workshop
University of Sussex, 9th/10th September 1998

Registration Form

Name _____ (Sex - M/F)

Institution _____

Address _____

_____

_____

Postcode _____

email _____

Please tick as appropriate:

☐ I will be attending the EEUG Workshop on the 9th and 10th September 1998, require overnight accommodation on the 9th and enclose a cheque for £66, made payable to EEUG, to cover the cost of the workshop, dinner, accommodation, breakfast, lunch, tea and coffee.

☐ I will be attending the EEUG Workshop on the 9th and 10th September 1998, require overnight accommodation on the 9th and enclose an official institution order form or number, which will be invoiced prior to the Workshop by EEUG for £66, to cover the cost of the workshop, dinner, accommodation, breakfast, lunch, tea and coffee.

☐ I will be attending the EEUG Workshop on the 10th September 1998 only and enclose a cheque for £30, made payable to EEUG, to cover the cost of the workshop, lunch, tea and coffee.

☐ I will be attending the EEUG Workshop on the 10th September 1998 only and enclose an official institution order form or number, which will be invoiced prior to the Workshop by EEUG for £30, to cover the cost of the workshop, lunch, tea and coffee.

☐ I will require a vegetarian menu

Cheques should be made payable to "EEUG".
Please send payment documentation and this form, AS SOON AS POSSIBLE, and at the latest by 21st August to:

Dr Steve Harrold, EEUG Treasurer,
Department of Electrical Engineering & Electronics,
PO Box 88, UMIST, Manchester, M60 1QD.
(*email:* s.harrold@umist.ac.uk)

Receipts will be distributed at registration on the 10th September.
The EEUG is not VAT registered.

CANCELLATION DETAILS

If you reserve a place but fail to attend the Workshop without cancelling your reservation before 1 September 1998, we reserve the right to retain or invoice you for the full fee, to cover the costs incurred.