EEUG News

The newsletter for Educational Electronic Computer Aided Design users

Volume 13 No 2 July 2000 *Editor: Steve Quigley (S.F.Quigley@bham.ac.uk)*

News from the ECAD Educational User Group Committee

In this issue

CHAIRMAN'S WELCOME

Welcome to the latest edition of the EEUG Newsletter.

The final arrangements are now being put in place for the September workshop to be held in Sorby Hall at the University of Sheffield on the theme of "Embedded Systems and Hardware/Software co-design". As you will see from the attached information your Committee has put together what promises to be an interesting and stimulating programme. I hope you already have the date on 6/7th September in your diary and would urge you to send your registration application as soon as possible so that we can have a successful meeting. After all, it is only the input of its members that can ensure the continuation of the EEUG. We will also be seeking your views on future workshop topics at the meeting.

Both Steve Quigley and myself are coming to the end of our terms of office on the committee. In fact, because of the change in timing of the AGM from January to September we have both completed more than the usual three years! I must particularly thank Steve for his excellent work during that time. I would also like to thank the members of the committee for the support they have given me in my role as Chairman. We are therefore seeking two new committee members, one of whom will be the next Newsletter editor. If you know of anyone, including yourself, who would be interested in contributing to the work of the EEUG then please contact either myself or any other member of the committee. In the meantime I look forward to meeting you again or for the first time in Sheffield in September.

Dr Mike English
EEUG Chair
School of Engineering & Information Technology
University of Sussex
(m.j.english@susx.ac.uk)

EEUG AGM

The year 2000 Annual general meeting of the EEUG will be held at the next Workshop on 7th September2000. The Agenda will be:

1. Chairman's Report.
2. Treasurer's Report.
3. Committee Member elections.
5. Any Other Business.

Anyone wishing to add further items to the Agenda should contact the Secretary (Dr.Margaret Fraser, Robert Gordon's University) before 1st September2000.

THE COMMITTEE

Chair: Mike English (m.j.english@sussex.ac.uk)
Secretary: Margaret Fraser (m.l.fraser@rgu.ac.uk)
Treasurer: Tim Forcer (tmf@ecs.soton.ac.uk)
Newsletter Editor: Steve Quigley (s.f.quigley@bham.ac.uk)

Other committee members:

- David Holding (d.j.holding@aston.ac.uk)
- Jon Travis (j.r.travis@shu.ac.uk)
- David Milford (d.milford@bristol.ac.uk)
- Jas Singh (j.singh@leeds.ac.uk)

Mike English and Jon Travis are the RAL MSC Advisory members.

RAL/EEUG ADVISORY COMMITTEE

The RAL/EEUG advisory committee met on 22nd June 2000 at the Cosener's House in Abingdon. Those present were John McLean and John Morris representing RAL with Mike English and Jon Travis representing EEUG. The main topics discussed were provision of low-end tools, scheme entry costs, design with integrated test, cycle accurate simulation of IP blocks, licence arrangements beyond the year 2000 and design synthesis from C. Current and future developments in Europractice were put in the context of the EU Framework 5 programme and this indicates a minimum guaranteed further 2½ years software support from RAL. The RAL website at http://www.te.rl.ac.uk/europractice/ contains information on the current situation.

At the September workshop at Sheffield University John McLean will present an update on any developments and RAL support staff will be present with demonstration software in their roadshow exhibition. This will present a good opportunity to ask any questions and gain information face-to-face.

Members of EEUG are reminded that the Advisory Committee exists to represent the views of the user community and so any issues which you wish to have raised should be communicated to either Mike English or Jon Travis.

Educational ECAD User Group
Autumn Workshop 2000
University of Sheffield, 6 - 7 September 2000

Embedded Systems and Hardware/Software co-design

The 24th EEUG Workshop will be held in Sorby Hall at the University of Sheffield on the 6th and 7th of September 2000. This workshop is intended to provide an opportunity to find out about current and recent projects in academic institutions addressing Embedded Systems design issues, whether as part of taught courses, for individual or group design projects, or in support of these areas.

The following presentations have been confirmed:

- **Hardware/Software Co-Design: A System-Level Approach**, *Robert Self, Martin Fleury, Andy Downton (University of Essex)*
- **Virtual Prototyping of Electronic Systems**, *Antony Kavassis, Phil Watten, Paul Lister, Martin White (University of Sussex)*
- **Applications of CoWare**, *Mark Willoughby (RAL)*
- **The real-time debug of embedded systems using dynamic on-chip data analysis**, *Geoff Lawday (Buckingham Chilterns University College)*
- **Reflections on PPF: New directions in constructing high specification image processing and multimedia embedded systems software**, *Martin Fleury, Andy Downton (University of Essex)*
- **SoftPIC - the disembedded microcontroller**, *Tim Forcer (University of Southampton))*

The RAL Roadshow will be demonstrating relevant EDA tools during coffee breaks and over lunch on the Thursday and in the afternoon John McLean will give an update on Europractice Software Services for the academic community. There will also be an update on the EDEC CAL software from Peter Hicks.

The cost for overnight attendees will be £66, which includes dinner and accommodation on the 6th and breakfast, lunch, tea and coffee on the 7th September. The cost for attending only for the day on the 7th will be £35, which includes lunch, tea and coffee. We have managed to hold our prices at last year's level.

Please post or email the following form, with payment documentation, to the EEUG Treasurer (Tim Forcer - tmf@ecs.soton.ac.uk), in order to register for the workshop.

Please circulate this information to your colleagues. We hope you will be able to join us in Sheffield for what promises to be a very interesting workshop.

Dr Mike English
(on behalf of the EEUG committee)

Educational ECAD User Group Workshop

Sorby Hall

University of Sheffield

6/7 September 2000

Embedded Systems & Hardware/Software Co-design

Provisional Programme

Weds 6th September

4.00 - 6.00 p.m.	Registration desk open at Sorby Hall
7.00 for 7.30 p.m.	Dinner
8.30 p.m.	Talk and demonstration of software by Embedded Systems Limited (ESL).
	Bar

Thurs 7th September

7.30 - 8.30 a.m.	Breakfast
8.45 a.m.	Registration
9.25 a.m.	Chairman's Welcome - *Mike English (University of Sussex)*
9.30 a.m.	**Hardware/Software Co-Design: A System-Level Approach** *Robert Self, Martin Fleury, Andy Downton (University of Essex)*
9.55 a.m.	**Virtual Prototyping of Electronic Systems** *Antony Kavassis, Phil Watten, Paul Lister, Martin White (University of Sussex)*
10.20 a.m.	**Applications of CoWare** *Mark Willoughby (RAL)*
10.45 a.m.	Coffee & RAL Roadshow
11.15 a.m.	**The real-time debug of embedded systems using dynamic on-chip data analysis** *Geoff Lawday (Buckingham Chilterns University College)*
11.40 a.m.	**Reflections on PPF: New directions in constructing high specification image processing and multimedia embedded systems software** *Martin Fleury, Andy Downton (University of Essex)*
12.05 p.m.	**SoftPIC - the disembedded microcontroller** *Tim Forcer (University of Southampton)*
12.30 p.m.	Lunch & RAL Roadshow
2.00 p.m.	EEUG Annual General Meeting
2.15 p.m.	EDEC update - *Peter Hicks (UMIST)*
2.35 p.m.	RAL MSC update - *John McLean*
3.15 p.m.	Tea & Close

ABSTRACTS FOR EEUG WORKSHOP, SEPTEMBER 2000, SHEFFIELD.

Hardware/Software Co-Design: A System-Level Approach
Robert Self, Martin Fleury, and Andy Downton, University of Essex.

Consumer demand for sophisticated real-time multimedia and mobile communications, enabled by continued advances in semiconductor technology, have led to a rapid increase in embedded system complexity. However, limitations in today's design methods and tooling hamper the designer's ability to deliver next-generation applications in a timely and cost-effective manner. This presentation examines advances in CAD and co-design tools by reviewing the co-design methodology adopted by CoWare and the SystemC approach to hardware synthesis. In addition, we report our experience of the Handel-C hardware compiler and the Ptolemy design and simulation environment tools. While these tools improve productivity by facilitating hardware and software concurrent engineering and raise abstraction levels in order to manage implementation complexity they fail to address the broader issue of system architectural design. We contend that a structured top-down approach is needed in order to develop robust systems from the diverse range of ASIC, programmable logic, and microprocessor platform options now available to engineers. We conclude by presenting our ideas on system architecture and methodology, which we believe will fill this system design gap.

Virtual Prototyping of Electronic Systems
Antony Kavassis, Phil Watten, Paul Lister and Martin White, University of Sussex.

This presentation gives a brief introduction to virtual prototyping applied to electronic systems and takes a look at our current direction. For some time the Centre for VLSI and Computer Graphics has been using high-level design techniques in the development of 3D graphics ASICs and FPGAs. This has led to a research thread in the area of prototyping of electronic systems. Based on our early work with an algorithmic-level development platform targeted at graphics, DPX has been developed to provide a high-level electronic prototyping environment using C++. We are extending this to provide a virtual environment for conceptual prototyping.

Applications of CoWare
Mark Willoughby, RAL MSC.

CoWare is a true Hardware-Software Co-Design tool that enables the user to specify a system-level description in a super-set of C. Exploration of various partitioning strategies of functional blocks between hardware and software can be successively tried and refined. The program automatically creates the software and hardware to implement the interfaces between blocks, prior to logic synthesis using conventional synthesis tools. CoWare via RAL ships with ARM7 processor target that is fully supported by additional Design Signoff Models and routes to fabrication via Alcatel Microelectronics. Similar flows for FPGAs will be supported when commercially available.

The real-time debug of embedded systems using dynamic on-chip data analysis
Geoff Lawday (Tektronix Reader in Measurement), Buckingham Chilterns University College.

Software and hardware design has become more efficient as development tools and simulators have improved in functionality. However, the software/hardware integration phase of embedded system development has increased in duration owing to the increased complexity and speed of modern embedded processors. The presentation describes one particular solution to this challenge. This is the use of a combination of debug tools that make use of the dynamic data acquisition facilities that microprocessor manufacturers have recently implemented. It is hoped that a demonstration will be included.

Reflections on PPF: New directions in constructing high specification image processing and multimedia embedded systems software
Martin Fleury and Andy Downton, University of Essex.

Parallel computing is still a necessity for those embedded systems such as target-tracking radar where throughput and/or latencies are otherwise too great. Product lifecycles of over ten years and microprocessor lifecycles of less than five years imply that a portable, scalable design is paramount. PPF (Pipelined Processor Farms) is a generic approach to top-down design of embedded parallel systems whose lessons remain relevant but which is being adapted to increasing hardware multiplicity. This paper will review the recent PSTESPA research project that aimed to systematize the construction and performance analysis of parallel computing systems with homogeneous processors. The presentation will look forward to the two-level multicomputer in which the processor interconnect is separated from the compute engine which might over time be choice of RISC, DSP, FPGA, or in part ASIC. It is proposed that the parallel software component is a way of encapsulating algorithms, parallel structure, and varying hardware granularity in a way convenient for system prototyping/codesign. PSTESPA as a project was interested in toolkits and it remains important to provide an infrastructure for testing at the system level.

SoftPIC - the disembedded microcontroller
Tim Forcer, University of Southampton.

Although the Microchip PIC is very popular with hobbyists and experimenters, and its Harvard architecture has attractions for introductory teaching of microprocessors, it is not widely used for practical work relating to such teaching because the actions of the processor are hidden behind the IC's ports. Since 1998, Southampton University staff and third-year project students have been developing SoftPIC - an FPGA-based hardware emulation of a PIC. In AY 2000/1 this will be used to give first-year undergraduates practical experience of the behaviour of a simple RISC micro. The presentation will address the philosophies behind SoftPIC, some of the aims of the laboratory programme in which it will be used, and aspects of the practical realisation of a SoftPIC experimentation platform.

Educational ECAD User Group Workshop
Embedded Systems and Hardware/Software co-design
Sorby Hall, Sheffield University, 6/7 September 2000

Registration Form

Title and Name: _____ *(Sex - M/F)*

Institution: _____

Address: _____

_____

_____

Postcode: _____ *email:* _____

Please tick as appropriate:

[ ] I will be attending the EEUG Workshop on 6 and 7 September 2000, require overnight accommodation on the 6th and enclose a cheque for £66, made payable to "EEUG", to cover the cost of the workshop, dinner, accommodation, breakfast, lunch, tea and coffee.

[ ] I will be attending the EEUG Workshop on the 6 and 7 September 2000 and require overnight accommodation on the 6th and enclose an official institution order form or number, which will be invoiced prior to the Workshop by EEUG for £66, to cover the cost of the workshop, dinner, accommodation, breakfast, lunch, tea and coffee.

[ ] I will be attending the EEUG Workshop on the 7 September 2000 only and enclose a cheque for £35, made payable to "EEUG", to cover the cost of the workshop, lunch, tea and coffee.

[ ] I will be attending the EEUG Workshop on the 7 September 2000 only and enclose an official institution order form or number, which will be invoiced prior to the Workshop by EEUG for £35 to cover the cost of the workshop, lunch, tea and coffee.

[ ] I will require a vegetarian menu.

Please send payment documentation and this form by August 18 at the latest to:

Mr T M Forcer, EEUG Treasurer
Department of Electronics & Computer Science
The University
SOUTHAMPTON
SO17 1BJ
Fax: 023 8059 2053

Receipts will be distributed at registration.
In the event of cancellation after August 25 or non-attendance without cancellation we reserve the right to invoice costs incurred up to the full fee.

EEUG workshops are exempt from VAT. VAT invoices and receipts will not be issued.